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Designing an Ultra Low Power Digital-to-Analog Converter: A 8-bit 144nW 40MHz 90nm D/A

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ABSTRACT: In this paper an ultra-low power Digital-to-Analog Converter (DAC) for ultra-low power applications is presented. A number of techniques are used to reduce the power consumption and relatively boost the speed of the DAC. These techniques include low current source and mirrors besides using low-voltage design with the aid of supply voltage as low as 1v. The circuit is designed in 90nm CMOS technology and simulations show that the 8-bit DAC consumes almost 144nW, 176nW and 615nW at the speeds of 40MHz, 46MHz and 50MHz respectively, i.e. it minimally dissipates only 144nW. Lower values couldn't be obtainable due to negative effects of lower scaled current sources on circuit performance. Higher speeds can be achievable at the cost of more power dissipation. There salts show that the proposed DAC could seriously compete with other DACs in ultra-low power applications, having relatively higher speed in comparison to its counterparts.

***Keywords*:** D/A, Ultra Low Power, Low Voltage Design, 8-bit DAC, MOSFET, FOM, SFDR, RFID, INL, DNL.

INTRODUCTION

THE Digital-to-Analog Converter (DAC) is the vital building block in many control systems such as video signal processor, digital signal synthesizer, HDTV and LCD driver ICs (column- and gate-driver ICs) and also in modern wireless transceivers where a large number of auxiliary DAC's are used to control RF circuits (1)(2)(3). Yet, ultra-low power DACs (nW range) could have been used widely in RFID, Wireless Sensor Network (WSN) and any digital assisted analog circuit, which typically needs low sampling rate and on the contrary requires low power consumption and small area for cost savings.

Discrete Time Sampling and Amplitude Quantization are the two fundamental processes which occur in a typical sampled data system as first step in design of DAC (17)(18). Fig. 1 shows a real-time system, but for data analysis and many signal processing applications, the signal is digitized and never converted back to analog.

Many of the DACs in literatures are based on device scaling techniques, namely current scaling, voltage scaling and charge scaling (19)(20) . Current-mode D/A converters are intended for high speed applications (4), though it has also the potential of being utilized in low power application where speed is not the major concern. Presented architecture in this paper proves that not only the ultra-low power consumption can be obtained in current-mode DAC but also relatively higher speeds are achievable in comparison with other architectures.

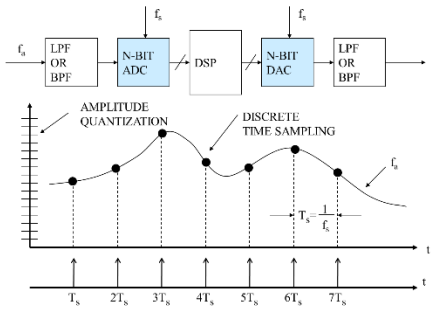

Figure 1. Discrete Time Sampling and Amplitude Quantization in design of DAC

In Fig. 2, we show a basic A/D and D/A with the analog input, voltage reference, sampling clock, digital output lines and the supplies. A DAC puts out a discrete voltage (or current) related to the digital code. The DAC cannot put out voltages between its codes. An ADC converts an analog signal to a digital code – the code is valid for a range of analog inputs (21). The schematic model is shown in Fig. 2.

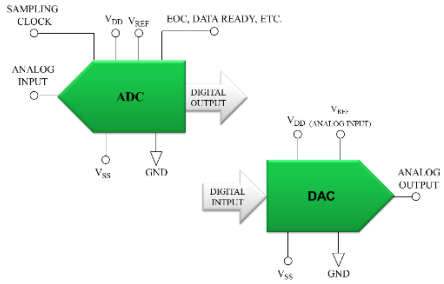

Figure 2. In this figure that is basic A/D and D/A with the analog input, voltage reference, sampling clock, digital output lines and the supplies are shown

Most ADCs today are used to process AC signals, and therefore there must be a sample-and-hold (SHA) function (22). Many ADCs of the 1970s required external SHAs, but today the function is built in to practically all ADCs. This allows the ADC to be completely specified for DC and AC performance, and the user does not need to worry about interfacing a discrete SHA to a separate ADC (encoder). Four key ADC Market segments:

- Data Acquisition,
- Precision Industrial Measurement,
- Voice band and Audio,
- High Speed

High Speed implying sampling rates greater than approximately 10MSPS—although this line of demarcation is somewhat arbitrary. A 2MSPS 16-bit SAR ADC is definitely "high speed" in its class. A basic understanding of the three most popular ADC architectures is valuable in selecting the proper ADC for a given application.

Architecture of Proposed DAC

The basic idea of the current-mode DAC has depicted in Fig. 3, illustrating 8 current sources passing their currents through the resistor R which alters the weighted currents into a corresponding voltage. Supply voltage as low as 1v has been used for the circuit due to having least power consumption and the best performance. By selecting a 1.85nA for current I and adopting a large resistor of value 1MΩ for R this architecture simply could have a low power dissipation. Larger capacitor and therefore lower current of I can degrade the performance of the circuit significantly.

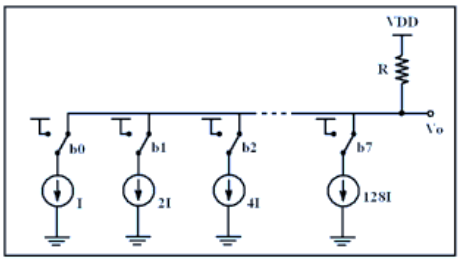

Figure 1.
Figure 3. Regular current-mode DAC

In Fig. 4 current sources and switches of the Fig. 3 have been replaced by current mirrors and MOSFETs, respectively. Input digital bits are applied to switching MOSFETs, allowing corresponding scaled currents to pass through R resistor. Thanks to weighted currents a weighted output voltage at node Vow ill is produced as well.

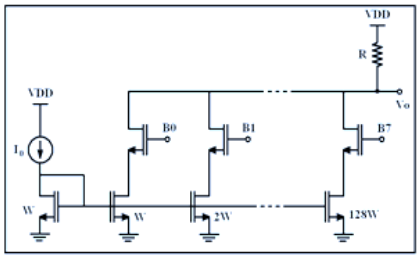

Figure 4. Current sources and switches of the Figure 1 has been replaced by current mirrors and MOSFETs

As the generations of MOSFETs scales down the channel-length modulation effect results in significant error of copying currents in current mirrors (5). As illustrated in Fig. 5, in order to suppress the short channel effects, cascade current sources has been used. The switches (B0-B7) are implemented to keep the capacitor voltage and current mirrors on. It will increase the speed, since the node capacitor does not need to recharge after switching. They are shown in Figure 3. Current from the current source is switched either to the output or to the power supply. Such a configuration helps to keep the current sources stable during switching. Moreover, the wider MOSFETs, the larger MOS capacitances will be produced, spending more time to discharge. They are there to keep the capacitor voltage and current mirrors on. It will increase the speed, since the node capacitor does not need to recharge after switching.

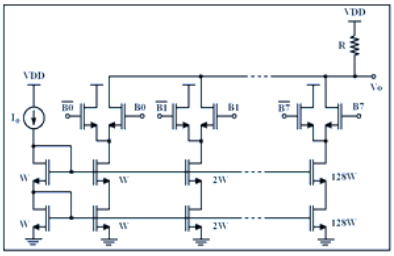

Figure 5. Architecture of the DAC and discharging MOSFETs plus cascade current sources

Simulation Results

When all input bits are high, all current sources will draw currents from the supply through resistor R, leading to shortest settling time and higher speed. Whereas the input code of 00000001 will produce the longest settling time, due to passing the least current through the resister R, and lowest speed. Therefore in order to evaluate the maximum speed of the DAC the preceding code had been applied to the DAC and consequently the maximum speed of 40MHz acquired only at the cost of 144nW power dissipation. Simulations show the INL and DNL of the DAC are -3.9~2.3LSB and ±2.7LSB, respectively, illustrated in Fig. 6 and Fig. 7.

Resolution is right proportional to power dissipation and inversely proportional to log Sfdr and Fom, that is, the more resolution the more power will be dissipated, undoubtedly. The more resolution the less Sfdr and Fom. The amount of such power consumption, Sfdr and Fom is simulated and demonstrated in Fig. 8. It shows that with the resolution of 10 bit the power dissipation will be up to 800nW. Simulations are performed at the voltage supply of 400mv.

Indeed for lower frequency the power consumption will be lower; this fact is illustrated in Fig. 9. It shows that this ADC consumes almost 76.8μW at 1GHz and 144nW at 40MHz. Table 1 demonstrates the results of simulations and makes a comparison with DACs in other papers.

Load is right proportional to Sfdr and inversely proportional to output range variation, the more Load the more Sfdr & less output range variation, undoubtedly. The amount of such Sfdr & output range variation is simulated and demonstrated in Fig. 10. It shows that with the Load of 16MΩ the Sfdr will be up to 900 & output range is less than 10mv and with the Load of 1MΩ the Sfdr will be to about 0.1 & output range is about of 400mv. finally Fom & Sfdr vs frequency, the simulation result is show in the Fig. 11, that see both is reduce with increased frequency.

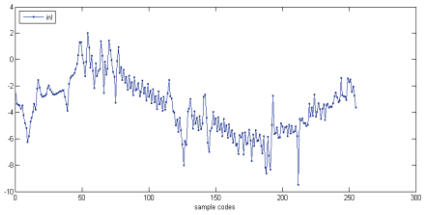

Figure 6. Integral nonlinearity@ 40MHz

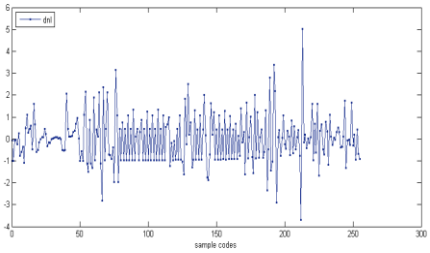

Figure 7. Differential nonlinearity @ 40MHz

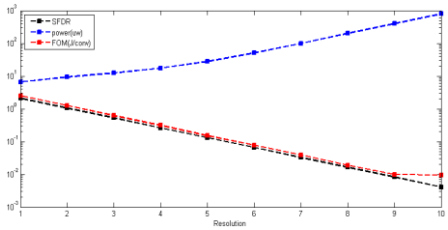

Figure 8. Power dissipation, FOM & SFDR vs. resolution

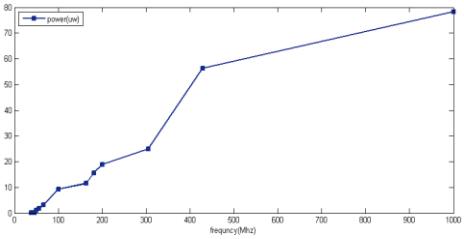

Figure 9. Power dissipation vs. sampling frequency

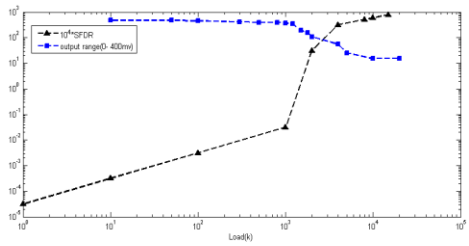

Figure 10. SFDR & output range vs. load

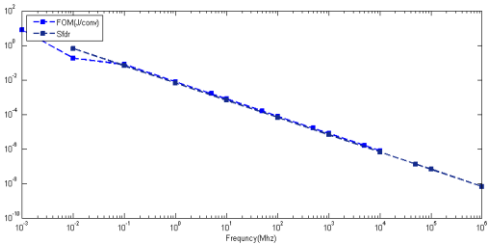

Figure 11. FOM & SFDR vs. frequency

CONCLUSION

In this paper, a low power current-mode D/A converter based on traditional architecture has been proposed. The DAC has been designed in 8 bit resolution and 40MHz speed at the cost of only 144nW power dissipation has been obtained. In order to reduce the total power consumption this DAC architecture has enjoyed an ultra-low current source and a large resister with the value of 1MΩ as well as a low voltage supply of 400mv. Simulation results show that the INL and DNL of this DAC are -3.9~2.3 LSB and -±2.7 LSB, respectively. Although DNL and INL show a wide range in terms of LSB, such a low power DAC could be utilized in passive RFID tags where low power dissipation outweighs precision. Simulations also depict that the proposed DAC has ultra-low power consumption and notice able speed in comparison with other DACs with the same range of power consumption. We can hope to make this system in future and we would like it feasible to upgrade.

References Parameters	6	7	8	10	11	12	14	15	16	This work
Power Supply	5.0 v	1.3v	1.8v	56mW @ 1.2V	1.1/2.5v	3.3v	1.2v	3.3v	-4.0	1.0v
Power Consumption	252 µW	10.6 mW	1.01 mW	72mW @ 2.5V	≤750 mW	10mw	660uw	40mw	0.95/1.4w	144nw
Sampling Rate	2 MHz	160 MHz	/ MHz	1.25 GS/s	56 GS/s	10 MS/s	8MHZ	-	28/32 GS/s	40 MHz
Technology	0.5µm	90nm	-	90 nm	65 nm	0.5µm	0.13µm	0.18 µm	1µm HBT	90 nm
INL (LSB)	±1	±0.6	1.57	+1.0/1.2	-	±0.3	-	±1.0	+0.97/-0.06	-3.9~2.3
DNL (LSB)	±0.1	±0.6	0.12	+0.45/0.5	-	±0.22	-	±0.8	+0.049/-0.17	±2.7
Resolution	9	12	8	12	6	8	16	12	6	8

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